Design and Optimisation of MEMS Capacitive Accelerometer

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Abstract

A micromachined accelerometer based on an area variation capacitive sensing for more applications was developed, in this case, we will describe and improve in this work the efficacy as well as the sensitivity of a capacitive accelerometer based on an area of variation capacitive sensing considered as a micro system electro mechanical (MEMS) available and realizable. However, the simulation was performed using *MATLAB* as software used in complicated situation with an optimization of the several parameters of accelerometer and a single direction, which is consisted with mobile fingers and fixed fingers, as two springs which ensures the damping of the system. The general concept, main design considerations and performance of the resulted accelerometer was optimized and elaborated in order to obtain a good improvement.

1. Introduction

The Micro Electro Mechanical System (MEMS) technology device design optimization is becoming an interesting and important research issue. However, various efforts on MEMS device design optimization and automation have been made as modeling and simulation of a capacitive micromachined accelerometer.

Compatibility with conventional CMOS provides advantages high yield and fast prototyping that should be adjustable and transferable to any CMOS foundry.

In this work, we present the difference and the relationship between the design optimization of a capacitance folded beam MEMS comb accelerometer device and the device sensitivity such as beam width, beam length, mass width. Based on the analysis, an optimized design of the MEMS comb capacitive accelerometer device is suggested.

2. CMOS micromachining process

The CMOS (complementary metal oxide semiconductor) micromachining accelerometer uses high technology, are made from custom processes combining polysilicon surface micromachining and electronic circuits processes [1]. It is fabricated using three-metal 0.5 μm n-well CMOS process through MOSIS [2]. After the fabrication, two dry etch steps, shown in figure1, are used to define and release the structure. Figure.1.a shows the cross section of the chip after regular CMOS fabrication. In the first step of post processing as shown in Figure.1.b, dielectric layers are removed by an anisotropic CHF_3/O_2 reactive-ion etch (RIE) with the top metal layer acting as an etch resistant mask [3].

After the sidewall of the microstructure is precisely defined, an isotropic SF_6/O_2 (RIE) is performed to etch away the bulk silicon and release the composite structure as shown in Figure.1.c [4]. Layout in the metal layers is designed to form beams, plates, and electrostatic comb fingers. Material property values for the composite structures include a density of 2300 kg/m^3 and a Young's modulus of 62 GPa.

Electrically isolated multi-layer conductors can be routed in the composite structures, enabling more design options (compared to homogeneous conductor structures). For example, electrically decoupled sensing and actuating comb fingers may be built on the same structure and full-bridge capacitive differential and common centroid comb-finger designs can be readily implemented [2].

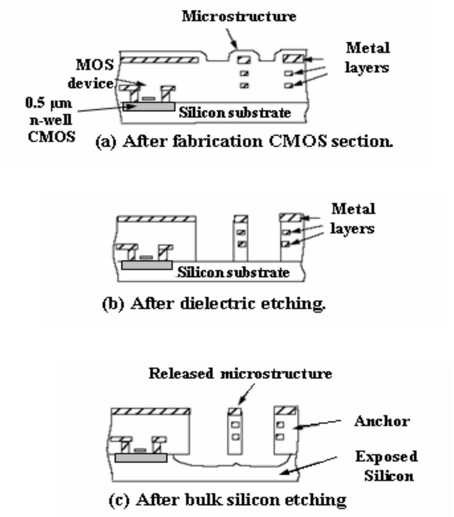

Figure 1.